

Data Sheet

# VIAVI

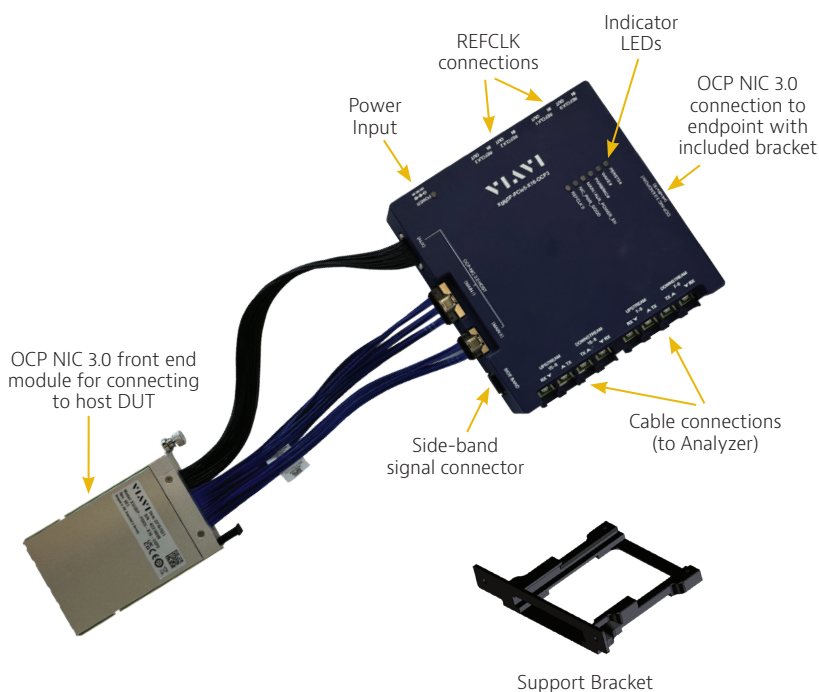
## Xgig 16-lane OCP3 Interposer

for PCI Express® 5.0

Provides a tap of host-system PCIe signals to OCP NIC 3.0 devices for input to the VIAVI Analyzer

VIAVI Solutions Xgig5P-PCIe5-X16-OCP3 Interposer is optimized for developing, debugging and performance-tuning OCP NIC 3.0 devices used in data centers. The OCP-NIC 3.0 specification was created by the Open Compute Project® to define a data center optimized form factor for PCIe devices. Bidirectional PCIe 5.0 protocol data on up to 16 lanes can be captured at 32 GT/s for analysis. The Interposer is designed to support 1 link of 16 lanes, 2 links of 8 lanes or 4 links of 4 lanes with proper licenses.

This Interposer uses high-speed linear signal redrivers to buffer the system data signals across the Interposer between host system and OCP NIC 3.0 devices-under-test. This design ensures a clean signal is delivered to the Analyzer for reliable protocol capture and analysis.



### Key Features

- Operates up to 32GT/s, PCIe 5.0 data rates
- Downward compatible with PCIe data rates of 2.5, 5.0, 8.0G and 16GT/s
- Supports 1 link of 16 lanes, 2 links of 8 lanes or 4 links of 4 lanes with proper licenses
- OCP NIC 3.0 DUT (not supplied) plugs directly into the Interposer
- Data path uses high-speed linear redrivers to ensure good signal capture with little or no tuning
- Includes high-quality cables for Analyzer connection
- Supports Analyzer side-band signal capture and triggering with display in multiple formats
- The supplied power brick makes Interposer power independent of host system
- LEDs give quick indicators of power and status
- Size: Base Pod: 175 x 167 x 35 mm
- Works together with the VIAVI Xgig5P-PCIe5-X16 Analyzer/Exerciser/Jammer chassis platform
- Provides consistent, repeatable capture of link training, equalization negotiation and other data
- Supports error injection (jamming) for deep system analysis
- Supported by Xgig tool suite including Trace Control, Expert™ and Serialytics™

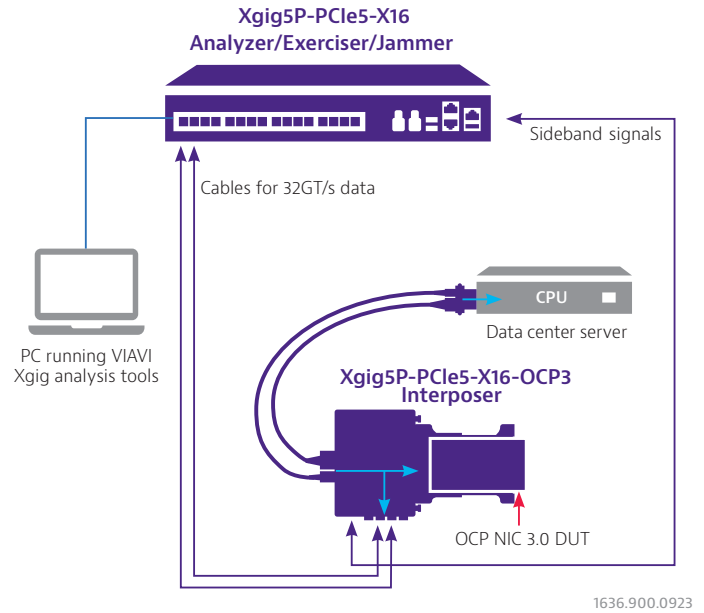
## Application

Working together with the VIAVI PCIe 5.0 Analyzer/ Exerciser/Jammer chassis, this Interposer enables debug and verification of new OCP NIC 3.0 PCIe controller ICs, new server designs, firmware tuning, validation of system BIOS and software, and for verification of manufacturing test.

To setup the interposer for operation, an OCP 3.0 NIC is inserted into the Interposer base pod. The Interposer front-end module is then inserted into the OCP NIC 3.0 bay of a data center server. To complete the test data path, the cables are attached connecting the Interposer with the VIAVI PCIe 5.0 protocol Analyzer/Exerciser/Jammer platform. Xgig analysis tools are loaded and run on a local or remote Windows PC. The block diagram to the right indicates the signal data path.

When operating in Analyzer mode, the DUT data is captured (tapped) from both the upstream and downstream data paths as inputs to the Analyzer. When operating in Analyzer/Jammer mode, data flows through the Analyzer and is modified between DUT devices. In Analyzer/Exerciser mode, data is sourced from the Analyzer chassis and connected to the server device under test via the Interposer.

VIAVI offers a variety of Interposer types for different PCIe system applications, including 4-, 8- and 16-lane CEM, U.2, E1, E3, M.2, Slimline and others.



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## Kit Contents

Item	Description	Qty
1	Xgig5P-PCIe5-X16-OCP3, 16-lane Interposer Base Pod	1
2	OCP NIC 3.0 Front-end module	1
3	Custom high-performance cables	8
4	Sideband cable (to analyzer)	1
5	Coax cable for optional clock	4
6	Power brick, 120/220 input, 12V/3A output	1
7	Bracket kit	1
8	Quick Start Guide	1

## Ordering Information

Part Number	Description
Xgig5P-PCIe5-X16-OCP3	Xgig 16-lane OCP3 Interposer for PCIe 5.0
Xgig-Intpsr-C-Hx (x=1, 2, 3, 4)	x-year extended hardware warranty



Contact Us **+1 844 GO VIAVI**  
(+1 844 468 4284)

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visit [viasolutions.com/contact](https://viasolutions.com/contact)

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